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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,815	12/30/2003	Andrew S. Grover	42.p18167	9370

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,815	GROVER, ANDREW S.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-12 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12,14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 October 2006 has been entered.

Status of Claims

2. Claims 1-6, 8-12, and 14-18 are pending in the Application.

Claims 1, 8, and 14, have been amended.

Claims 7, 13, and 19 remain cancelled.

Claims 1-6, 8-12, and 14-18 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 15 November 2006 in response to the office action mailed on 18 August 2006 have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 8-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, the machine readable medium as recited in these claims is directed to both statutory (i.e. EEPROM) and non-statutory (i.e. carrier waves) subject matter. Please refer to paragraph 0021, lines 1-7 of Applicant's original specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-6, 8-12, and 14-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 8 and 14 recite the limitation "the data being available on the memory unit after the system has been rebooted" in lines 10-11. There is insufficient antecedent basis for this limitation in the claim, as it is unclear if “the data” is referring “the data” including data identifying the predetermined event, or the data itself that identifies said event (i.e. is the data which includes data being claimed, or the data included in the data being claimed here?). The former is assumed.

The remaining claims are rejected for inheriting the deficiencies of each of their respective base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 6, 8, 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortin et al., hereinafter Fortin (US PG Publication 2004/0003223 A1, in view of Douglis et al., hereinafter Douglis (US Patent 5,481,733) and in further view of Applicant's admitted prior art.

As for claims 1, 8 and 14, Fortin teaches a system comprising of:

a processor (Fig. 2, element 120);

a non-volatile cache coupled to the processor (Fig. 2, flash memory 200 can be located as a separate component (as shown by element 202) which is coupled to the processor via the system bus (element 121) – paragraph 0030, all lines). Also note, the flash memory (element 200) can also serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used

as a cache by the system to reduce the access burden of the hard disk; and

a machine readable medium having stored thereon a set of instructions (the system memory as illustrated in Fig. 2, element 130, contains RAM and ROM sections which contain the OS, application programs, boot code, etc. which are used by the system to execute all system functions).

Though Fortin teaches storing configuration data in the non-volatile memory, he fails to defining a predetermined event, the occurrence of which causes a spin-down of a hard disk, detecting the occurrence of the event and in response to the event, spinning down the disk and storing historical hard disk performance data.

Douglis teaches a method for managing the power distributed to a disk drive in a laptop computer, wherein a state table is stored in a memory, the memory being used to store performance data of the hard disk drive. Based upon a history of disk accesses by a user, the number of transitions between each pair of states is counted and stored in memory. The information is used to predict a future period of inactivity in order to conserve power to the disk drive (see abstract).

Douglis further teaches the historical hard disk performance data as consisting of data identifying events the produced a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up. Douglis teaches spinning down a hard disk drive when it is unlikely to be accessed in the near future (col. 8, lines 15-25). A

prediction is made based on the past history of disk activity, which is stored in the memory. If the most likely time for the disk to be accessed is greater than a preset threshold, then the disk is spun down (col. 8, lines 38-50). In the case of this power down, historical data is recorded (i.e. period of inactivity) which indicates that the power down occurred because the inactivity data stored indicates the threshold has been exceeded. The method Douglis teaches includes quantizing the periods of inactivity into states, therefore periods of activity, and inactivity can be recorded to more efficiently power down the system (col. 8, lines 52-63). The states that are recorded to include predicting when to spin the drive back up based on the predicated next access (col. 10, lines 46-59). In other words, the system works to anticipate how long the drive should stay powered down before its spun back up based on the historical data.

Additionally, neither Douglis nor Fortin either, alone or in combination, teach storing data identifying the predetermined event as a cause of a spin-down of the hard disk as recited by Applicant in these claims.

This limitation however fails to render the claims patentable distinct, as storing historical hard disk data about event that result in spinning down of a hard disk is prior art, based on Applicant's own admission in the background of the original specification (see paragraph 0004, all lines). Pursuant to MPEP § 2129, "[w]here the specification identifies work done by another as "prior art", the subject matter so identified is treated as admitted prior art."

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance

data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25). Note, though Douglis's teaches his system as being applied to a laptop computer, it is well known to one of ordinary skill in the art that power conservation is valuable to many different computing systems, not just to a laptop computer environment.

It would have been obvious to one or ordinary skill in the art at the time of the invention for Fortin to include storing the cause of spinning down a hard disk into his own system used to store configuration data. By doing so, Fortin could benefit from an improved power management policy capable of not only recording when a drive is powered down, but also its cause.

As for claims 2, 9 and 15, Fortin teaches the non-volatile cache as being a cache for the hard disk (the flash memory (element 200) can serves as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk).

As for claim 6, Douglis teaches using the historical hard disk performance data to implement a power management policy of the hard disk (the predicated period based on

historical accesses by the user ultimately leads to spinning down the disk in order to put it in low power mode (see abstract)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25).

7. Claims 5, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin, Douglis and Applicant's admitted prior art as applied to claims 1, 8 and 14 above, and in further view of Sanada et al., hereinafter Sanada (US PG Publication 2001/0002173 A1).

As for claims 5, 12, and 18, though the combined teachings of Fortin, Douglis and Applicant's admitted prior art meet all the limitations of the base claims, they fail to further include the non-volatile memory consisting of a thin film electronic memory.

Sanada however teaches a semiconductor storage device and production method thereof wherein he specifically teaches manufacturing a flash memory via thin film processing techniques (paragraph 0071, all lines).

It would have been obvious to one of ordinary skill in the art at the time for Fortin in view of Douglis and in further view of Applicant's admitted prior art to include his cache memory as consisting of thin film in order to have a more optimized memory that

is capable of uniform data erase in a group of memory cells with a reduced number of cell in which the data erase is excessively performed as taught by Sanada (paragraph 0039, all lines).

8. Claims 3-4, 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin, Douglis and Applicant's admitted prior art as applied to claims 1, 8 and 14 above, and in further view of Chou et al., hereinafter Chou (US PG Publication 2005/0055481 A1).

As for claims 3-4, 10-11 and 16-17, though the combined teachings of Fortin, Douglis and Applicant's admitted prior art meet all the limitations of the base claims, they fail to further teach the memory include a form factor of a Mini Peripheral Component Interconnect Express (mini-PCI express) card, and interface. It is worthy to note Fortin does discuss his flash memory as a separate component such as a PC slot card, just not implemented as a mini-PCI express – see paragraph 0017, lines 1-9.

Chou however teaches a Flash drive/reader with serial-port controller and flash-memory controller mastering a second RAM-buffer bus parallel to a CPU bus. In his disclosure, Chou teaches connecting a system CPU to flash-controller, which accesses an attached flash memory, which is further connected to serial engine (see Fig. 4). This connection can be implemented in part by a mini-PCI Express (paragraph 0055, all lines). Also note, a Mini-PCI express card, must inherently posses a Peripheral Component Interconnect Express interface in order to function (i.e. communicate with the system).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin in view of Douglis and in further view of Applicant's admitted prior art to further include a mini- PCI Express in order to increasing data throughput via the buffering and a second data bus as taught by Chou (paragraph 0024, all lines).

9. Claims 1, 2, 6, 8, 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortin (US PG Publication 2004/0003223 A1), in view of Douglis (US Patent 5,481,733) and in further view of Miyano (US PG Publication 2005/0219733 A1).

As for claims 1, 8 and 14, Fortin teaches a system comprising of:

a processor (Fig. 2, element 120);

a non-volatile cache coupled to the processor (Fig. 2, flash memory 200 can be located as a separate component (as shown by element 202) which is coupled to the processor via the system bus (element 121) – paragraph 0030, all lines). Also note, the flash memory (element 200) can also serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk; and

a machine readable medium having stored thereon a set of instructions (the system memory as illustrated in Fig. 2, element 130,

contains RAM and ROM sections which contain the OS, application programs, boot code, etc. which are used by the system to execute all system functions).

Though Fortin teaches storing configuration data in the non-volatile memory, he fails to defining a predetermined event, the occurrence of which causes a spin-down of a hard disk, detecting the occurrence of the event and in response to the event, spinning down the disk and storing historical hard disk performance data.

Douglis teaches a method for managing the power distributed to a disk drive in a laptop computer, wherein a state table is stored in a memory, the memory being used to store performance data of the hard disk drive. Based upon a history of disk accesses by a user, the number of transitions between each pair of states is counted and stored in memory. The information is used to predict a future period of inactivity in order to conserve power to the disk drive (see abstract).

Douglis further teaches the historical hard disk performance data as consisting of data identifying events the produced a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up. Douglis teaches spinning down a hard disk drive when it is unlikely to be accessed in the near future (col. 8, lines 15-25). A prediction is made based on the past history of disk activity, which is stored in the memory. If the most likely time for the disk to be accessed is greater than a preset threshold, then the disk is spun down (col. 8, lines 38-50). In the case of this power down, historical data is recorded (i.e. period of inactivity) which indicates that the power

down occurred because the inactivity data stored indicates the threshold has been exceeded. The method Douglis teaches includes quantizing the periods of inactivity into states, therefore periods of activity, and inactivity can be recorded to more efficiently power down the system (col. 8, lines 52-63). The states that are recorded to include predicting when to spin the drive back up based on the predicated next access (col. 10, lines 46-59). In other words, the system works to anticipate how long the drive should stay powered down before its spun back up based on the historical data.

Additionally, neither Douglis nor Fortin either, alone or in combination, teach storing data identifying the predetermined event as a cause of a spin-down of the hard disk as recited by Applicant in these claims.

Miyano however teaches a recording medium device, which maintains a log of data, which is used to determine why (i.e. cause) a particular drive powered down (i.e. failed) – paragraph 0160 all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25). Note, though Douglis's teaches his system as being applied to a laptop computer, it is well known to one of ordinary skill in the art that power conservation is valuable to many different computing systems, not just to a laptop computer environment.

It would have been obvious to one or ordinary skill in the art at the time of the invention for Fortin to include Miyano's recording medium device into his own system used to store configuration data. By doing so, Fortin could benefit by exploiting the advantages of self-diagnosing a hard drive failure without the aid of a skilled worked as described by Miyano in paragraph 0002, all lines.

Claims 2, 6, 9 and 15 are rejected based on the claim mapping and motivation as set forth in paragraph 0006, *supra*.

10. Claims 5, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin (US PG Publication 2004/0003223 A1), Douglis (US Patent 5,481,733) and Miyano (US PG Publication 2005/0219733 A1) as applied to claims 1, 8 and 14 above, and in further view of Sanada et al., hereinafter Sanada (US PG Publication 2001/0002173 A1).

Claims 5, 12 and 18 are rejected based on the claim mapping as set forth in paragraph 0007, *supra*.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin in view of Douglis, in further view of Miyano to include his cache memory as consisting of thin film. By doing so, they would benefit by having a more optimized memory that is capable of uniform data erase in a group of memory cells with a reduced number of cell in which the data erase is excessively performed as taught by Sanada (paragraph 0039, all lines).

11. Claims 3-4, 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin (US PG Publication 2004/0003223

A1), Douglis (US Patent 5,481,733) and Miyano (US PG Publication 2005/0219733 A1) as applied to claims 1, 8 and 14 above, and in further view of Chou et al., hereinafter Chou (US PG Publication 2005/0055481 A1).

Claims 3-4, 10-11 and 16-17 are rejected based on the claim mapping as set forth in paragraph 0008, *supra*.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin, Douglis and Miyano to include a mini-PCI Express in order to increase data throughput via the buffering and a second data bus as taught by Chou (paragraph 0024, all lines).

Response to Arguments

12. Applicant's arguments with respect to claims 1-6, 8-12 and 14-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
1-30-07